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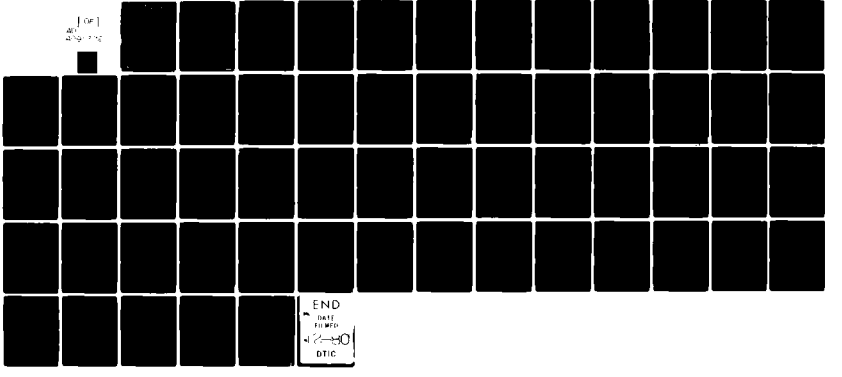

LEVEL II

DNA 5163T

RAM TECHNOLOGY STUDY

Mission Research Corporation
P.O. Box 1209
La Jolla, California 92038

3 January 1980

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Electrical performance and radiation hardness parameters of modern RAM technologies were compared for consideration in military hardened system applications. Semiconductor technologies considered included production dynamic n-MOS, statis n-MOS, CMOS, bipolar ECL developing CMOS/SOS and bipolar I^2L. For the production technologies CMOS and bipolar ECL are clear candidates for hardened systems with limited application for static n-MOS and very limited application for dynamic n-MOS.

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SECTION 1
INTRODUCTION

The evolution of complex microcircuits involves a variety of competing technologies, each with its own proponents and critics. In order to provide some basis for comparison of competing semiconductor technologies it is helpful to select a common complex function. The function selected for this study is that of a Random-Access-Memory (RAM). This function is realized in virtually every semiconductor technology either in production or research laboratories. The objective of this study is to gain some insight into the comparative advantages and limitations of these technologies within the limits of the common RAM function.

1.1 MEMORY ARRAYS

Random-Access-Memories are defined as those in which the access time to any memory location is independent of the initial memory location. This distinguishes RAM's from sequential memories such as magnetic tape, magnetic disk, bubble and semiconductor CCD's. All Random-Access-Memories have the capability of both reading and writing data into the memory array. Typically, RAM's are considered as monolithic semiconductor arrays in which read and write times are approximately equal. Characteristics of other types of read/write memories are presented in Table 1. The principal distinguishing characteristics are the time required to program new data into the array (write cycle time) and the ability of the array to retain the data after power is removed (volatility). The level of chip complexity is that of the most complex arrays in current production and is a rough measure of the limitations implicit in fabrication.

Table 1. Read/write memory characteristics.

Acronym	Description	Write Cycle Time	Data Retention	Chip Complexity
ROM	Read-Only-Memory	~ weeks	∞ , non-volatile	64 kbits (a,b)
PROM	Programable ROM	~ minutes	~ years	16 kbits (c)
EPROM	Electrically PROM (UV)	~ seconds	~ months	32 kbits (d)
EAROM	Electrically-Alterable ROM	~ ms	~ months	4 kbits (e)
RAM	Random-Access-Memory			
	Dynamic	~ µs	0, volatile	64 kbits (f) 16K (g)
	Static	~ µs	0, volatile	16K (h) , 4K (i)
	Magnetic Core	~ ms	~ years	wired components

a. Mostek 36000, AMI S4264, National 1NS8364, Signetics 2644: n-MOS
b. Harris HM 6388 (full mil temp.), Intersil 6364: CMOS
c. Signetics 82S190, Intel 3636, MMI 53LS1641
d. T.I. TMS 2532, Intel 2564, Motorola MCM68764: n-MOS
e. G.I. ER3400: MNOS
f. Mostek MK4164, Fujitsu MB4164: n-MOS
g. Fairchild 93483: bipolar
h. Intel 2116, T.I. TMS 4070: n-MOS
i. Fairchild F10470: bipolar; Harris HM 6543: CMOS

Data in the Read-Only-Memory is defined by the metallization pattern during chip fabrication. The stored data are non-volatile and a data change (write) requires the procurement of a new chip from the manufacturer with a different metallization pattern. The ROM represents the simplest storage of data and associated circuitry and represents the highest level of capacity in semiconductor memories.

The Programmable-Read-Only Memory is generally a bipolar array using diode or transistor elements with fusible-links for the memory elements. A user can program desired information by blowing fuses at selected locations (once). The write time is that necessary to set up the special equipment and deliver current pulses to each fuse location to be blown. Complexity is limited by the geometry and power dissipation of the peripheral bipolar circuits.

The Electrically-Programmable Read-Only Memory generally consists of a matrix of floating-gate MOS transistor elements. A user can program the array using electrical signals. Data can be mass-erased by ultraviolet (UV) exposure and the array can subsequently be re-programmed. Electrical programming must generally be done in an out-of-circuit fixture. Volatility is determined by the gradual charge loss in the floating gates.

An Electrically-Alterable Read-Only-Memory is a matrix of MNOS or floating-gate MOS transistor elements. For the MNOS arrays programming may be done in-circuit and data can either be erased in bulk or by individual words. Volatility is determined by the gradual redistribution of charge in the gate insulator of the memory transistors. The level of complexity is substantially limited by the fabrication complexities of the MNOS peripheral circuits.

Semiconductor Random-Access-Memories may be either dynamic or static arrays. In the dynamic arrays the stored information must be periodically refreshed to prevent loss. Dynamic memory cells are very small but

chip complexity is limited by the complexity in data transfer and refresh. Static RAM's do not require information refresh but do require more complex memory cells which limit array complexity. All semiconductor RAM's are volatile (i.e., all stored data are lost when power is removed). Power-down techniques can be used, however, to minimize power dissipation and retain stored data, or the RAM can be backed up with an EAROM to store the data as a power removal is sensed.

Outside of semiconductor memories, magnetic cores have been used for many years as computer memories. Generally cores have fallen behind semiconductor memories because of circuit volume, power dissipation and cost, but they have the advantage of non-volatility with Random-Access-Memory performance.

A general discussion of radiation effects on all types of read/write memories is beyond the scope of this study. It can be pointed out, however, that non-volatility during a radiation exposure is highly desireable and is generally defined as data retention. In general, all RAM's exhibit data retention up to the level where performance is compromised by permanent damage effects. The exception is radiation-induced latch-up which has been observed in bipolar RAM's. Data retention of core memories depends on the design of the associated circuitry. The cores themselves will retain data through the radiation exposure if not disturbed by the transient response of the electronics. EPROM's have virtually no radiation data retention capability. The ionizing radiation erases the stored information just as effectively as deliberate UV erasure. MNOS EAROM's have the potential for data retention but are limited by permanent damage effects on the MNOS and MOS transistor elements. Data stored in semiconductor RAM's can be upset by a high-intensity pulsed ionizing radiation exposure and have no intrinsic ability for data retention. Radiation-induced latch-up may also compromise operational memory performance. These issues will be discussed in much greater detail for semiconductor RAM's.

1.2 SEMICONDUCTOR TECHNOLOGIES

The scope of this study has been generally limited to n-MOS, CMOS and bipolar TTL/ECL RAM arrays. These are the dominant commercial RAM technologies as represented by a wide variety of both industrial and military products.

The basic element of the n-MOS arrays is the silicon-gate transistor element.[1] Source and drain regions are formed by diffusion and contacted with aluminum metallization. The gate conductor is doped amorphous silicon which also defines the gate alignment without overlap of the source or drain region. Ion-implantation techniques are used extensively to adjust the doping of the silicon gate and/or channel for threshold voltage adjustment. For an enhancement device there must be no channel conduction for zero gate-source bias. The positive gate-source bias necessary for conduction is defined as the threshold voltage, V_T. For a depletion mode device, channel conduction occurs at zero gate bias and the transistor is turned off by a negative bias (i.e., a negative value for threshold voltage). In silicon-gate n-MOS arrays. depletion mode transistors are used for switching elements and transmission gates.

The basic elements of CMOS arrays are n- and p-type MOS transistors configured in the basic form of an inverter or transmission gate.[2] Currently both aluminum-gate and silicon-gate CMOS arrays are in production. Silicon gate arrays are generally of higher density and performance compared to the older aluminum-gate technology. The substrate of the CMOS array is crystal silicon. The n-type transistors are formed in a previously diffused p-well which also provides junction isolation from the other transistor elements. One dimension in the evolution of CMOS arrays is the incorporation of n-MOS logic circuits and bipolar drive transistors on the same chip to gain advantages in switching speed and drive capability to supplement the CMOS advantages of very low power and high noise immunity.

The third major commercial technology are bipolar RAM arrays. Bipolar transistor elements are formed in a silicon substrate and isolated by reverse-biased p-n junctions. The cell forms of bipolar array have evolved from Transistor-Transistor-Logic (TTL) circuits and are presently trending to high density Emitter-Coupled-Logic (ECL) circuits. High density bipolar arrays also generally use some variety of sidewall oxide isolation and washed emitters to minimize transistor geometry and switching speed.[3]

Semiconductor technologies considered in less detail in this study include V-MOS, CMOS/SOS and I^2L. V-MOS is a process for forming n-MOS transistors on the sloped groove in the bulk semiconductor.[4] The process can be used to produce extremely small transistor elements and, used with conventional n-MOS transistors for transmission gates, high density, high performance arrays. V-MOS technology was put into production by AMI but has recently been withdrawn from production due to yield problems.[5] The technology is still potentially promising but is apparently not yet ready for full production.

CMOS/SOS is the fabrication of n- and p-MOS transistors in crystal silicon islands formed on an insulating sapphire substrate.[6] Complex CMOS/SOS arrays have been fabricated using either aluminum-gate or silicon-gate technology in both logic and memory arrays. The technology has the CMOS advantages of low power and high noise immunity with the additional potential advantages of high speed and cell density and radiation hardness. Unfortunately, processing difficulties and sapphire costs have prevented introduction into high-volume production. The technology is still promising and is currently under development in research laboratories and limited production.

While I^2L was originally proposed as a memory technology, its current success is only in complex logic arrays. The only I^2L-like memory currently in production is the Fairchild 93481 dynamic RAM.[7] The principal difficulty of I^2L memory cells is that all inverters require a ground ter-

minal which prevents the efficient realization of a transmission gate. The transmission gate is a key element in memory addressing circuits which enable the realization of large RAM's. Other advance bipolar technology forms are under development (e.g., Advanced Schottky Logic, Integrated Schottky Logic) but have not yet been realized in full production of complex memory arrays.

1.3 SCOPE

Critical parameters of Random-Access-Memories selected for comparison are: 1) chip complexity and size, 2) electrical switching response, 3) power dissipation, 4) noise immunity, and 5) radiation hardness. As might be expected, although relative ranking within each category can be established (while sometimes somewhat subjectively), no clear rank order can be established considering all performance parameters.

The highest density and array complexity of RAM technology is that of dynamic n-MOS. Best switching performance of the RAM's is that of the ECL arrays, closely followed by recently developed n-MOS arrays. Minimum power dissipation in standby or low data rates is clearly attained with CMOS technology. Operating at maximum data rates the power dissipation of all RAM technologies is relatively close, considering the variations in speed capability. Noise immunity is considered in terms of interface signals, system noise and alpha-particle induced soft errors. Generally CMOS and CMOS/SOS technologies are the best for overall noise immunity, bipolar and static n-MOS are comparable, and dynamic n-MOS limited because of system noise and soft-error susceptibility. Determination of ranking radiation hardness also involves a variety of considerations. In terms of permanent damage effects it appears that bipolar ECL leads the RAM technologies. The relative ranking of the other RAM technologies to permanent damage effects is CMOS, I^2L, static n-MOS and dynamic n-MOS. The best RAM technology for transient effect is CMOS/SOS, followed by bulk CMOS assuming processing to eliminate latch-up susceptibility. Logic upset levels of bipolar and static n-MOS technologies are comparable. Dynamic n-MOS arrays are the most susceptible to radiation-induced upset.

Exclusive of radiation hardness, it could be argued that the overall performance pace in RAM technology is currently set by dynamic n-MOS followed by static n-MOS, bulk CMOS and bipolar ECL-type arrays. This order is close to the inverse that could be argued for radiation hardness. This dichotomy will continue to exist but shouldn't get much worse. The total dose hardness of memories should stabilize at a failure level greater than about 1,000 rads(Si) rather than continue to decrease with increasing array capacity. Existing n-MOS designs are about at the limits in sensitivity for small, matched threshold voltages and threshold voltage margins will probably not be reduce in arrays of increased complexity. Development of low current static n-MOS and bipolar RAM cells will increase the RAM sensitivity to radiation-induced increase in junction leakage currents with some probable deterioration in radiation hardness.

SECTION 2

RAM ORGANIZATION AND CAPACITY

The organization of a semiconductor RAM is structured for specific applications with the universal goal of minimizing the number of external pins. Pins on the package are minimum for an n-word by 1-bit organization. Thus, a 16k × 1 memory would require 14 address pins and a single output pin (total = 15), in addition to power supply, ground and clock inputs. The n × 1 organization is useful for large memory systems but inconvenient for small microprocessor memories. Holding the memory size constant and increasing the word width would result in 16 pins for a 4k × 4 memory, 19 pins for a 2k × 8 memory and 26 pins for a 1K × 16 memory.

Increasing the word depth of the array increases the complexity and propagation delay of the address decoders with impact on the chip complexity and access time. Conversely, increasing the word width reduces decoder complexity but increases the number of output drivers with an increase in chip area due to the relatively large area requirements of each output driver. Variations in performance with memory organization are a strong function of specific semiconductor technology and circuit design such that general observations are difficult to define.

Minimizing the number of pins on the package is becoming more important because of limitations in semiconductor and subsystem packages for high performance, large memories. Lead impedance may be an important constraint in getting fast, low energy RAM signals from the chip to the package terminals as well as between memory and logic arrays.

For a given organization, the number of package pins can be reduced by multiplexing the address. Part of the address can be read and latched with the remainder of the address read just afterwards on the same terminals. This reduction in address pins can be an important advantage for large 16k × 1 or 64k × 1 semiconductor memories. Another scheme to minimize pins is to clock some of the address inputs as refresh for dynamic RAMs eliminating some of the dedicated clock inputs.

2.1 MEMORY CELLS

The first semiconductor memory cell was a single flip-flop, or bistable, circuit. A single bit of information was stored in the relative balance of "on" and "off" bipolar transistors in the circuit. The flip-flop cell is two cross-coupled inverters and can store information indefinitely as long as the power supply remains on. Stored information is lost when the power supply is turned off (volatile). The flip-flop cell is the basis for all static RAMs. As the technology has evolved new circuit elements, smaller element geometries and new cell designs now can be realized with 16,384 static memory cells on a monolithic semiconductor chip.

It is not necessary to have two cross-coupled inverters to store information. A single inverter will hold its logic state on its capacitances if it is electrically "disconnected" from the circuit. The information storage time will be determined by the charge leakage of the capacitances. In MOS technology the inverter cell can be disconnected by transmission gates and junction leakage currents are low enough to store information for several milliseconds. This dynamic logic concept was first realized in p-MOS shift registers. The evolving technology then split to the present charge-coupled-device (CCD) sequential memories and dynamic random-access-memories. The present production capacity of dynamic RAM's is at (or near) 65,536 bits (64 kbits) arrays.

In the evolution of RAM technology the size of the semiconductor chip has remained relatively constant (about 0.4 cm × 0.4 cm) and the increase in capacity has principally been in the reduction of the cell geometry. Much of this reduction has been due to improved photolithographic techniques and smaller element geometries, but substantial improvement has been obtained from circuit designs using fewer elements.

2.1.1 n-MOS Dynamic Memory Cell

The current standard dynamic RAM memory cell is the "one-transistor" cell. This has been an evolution from the three-transistor cell as shown in Figure 1.[8] Transistors Q1 and Q3 are transmission gates. With no gate bias the transistors are off and essentially represent an open switch. With a write select signal Q1 is turned on and the gate of Q2 is charged to the logic state of the write data bit. The capacitance, C, is the sum of the gate capacitance of Q2 and the drain-substrate capacitance of Q1. With Q1 off the charge on the capacitance would be retained forever except for junction leakage currents. The state of the memory cell is detected by turning on Q3 with the read select bias and sensing the "on" or "off" state of Q2 through the read data bit line as defined by the gate bias on Q2. The read process is almost non-destructive since the drain-source sense current does not strongly effect the gate charge.

Since the charge on the storage capacitance cannot be maintained indefinitely, stored data must periodically be sensed and re-written into the array (refresh). The time between refresh cycles is a function of the leakage currents which, in turn depend on the chip temperature, background gamma radiation, alpha particles and cosmic rays. Typical refresh periods, exclusive of radiation, are on the order of milliseconds.

The density of the dynamic array was improved by combining the read and write data bit lines into a single read/write (R/W) line. The

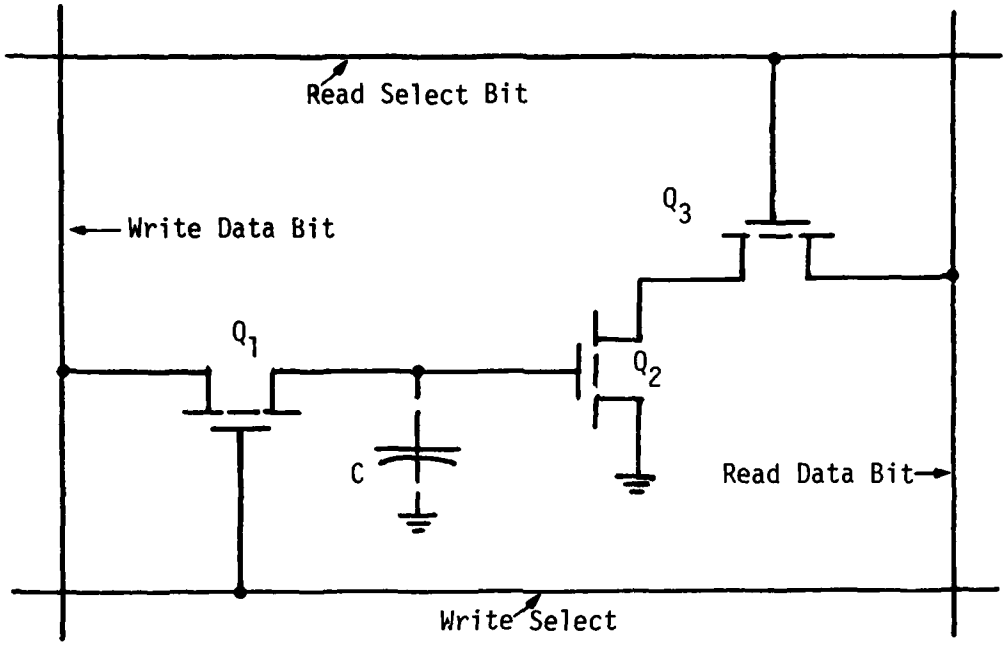


Figure 1. Three-transistor dynamic RAM cell, dual input output lines.

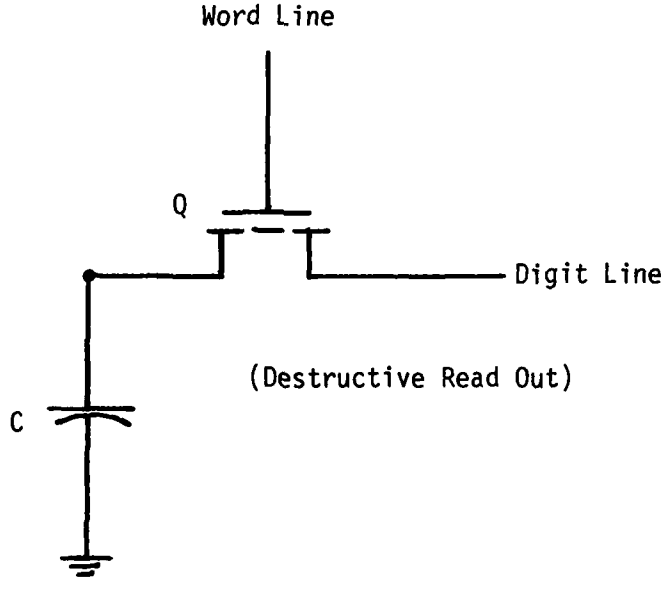
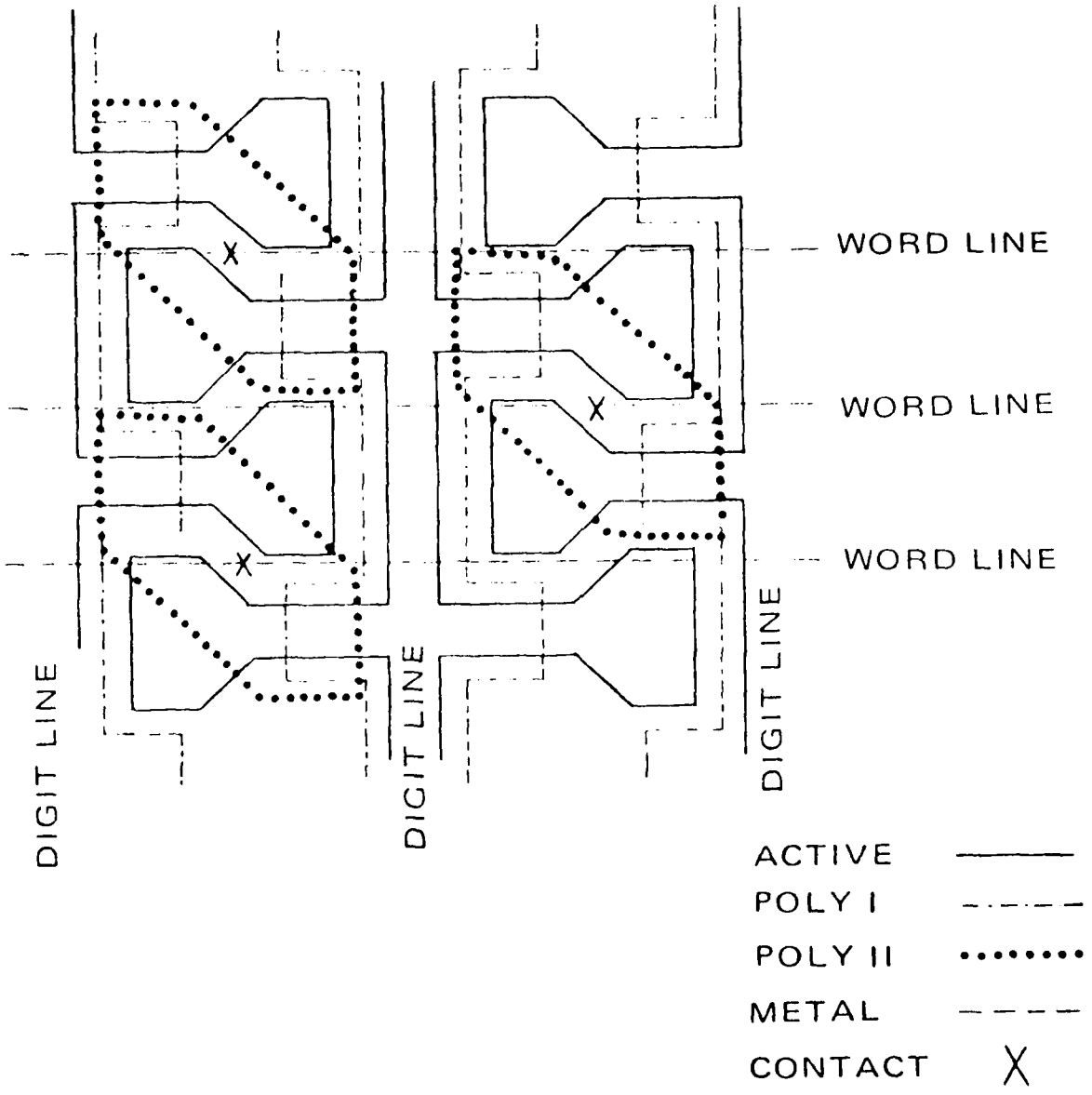


Figure 2. Single transistor (1-T) dynamic RAM cell.

major improvement in dynamic RAM technology was, however, the realization of the single transistor memory cell as shown in Figure 2.[8] In the 1-T memory cell the storage capacitor is an equally critical element and, formed by the sum of junction and oxide capacitances, typically requires the majority of the cell area. The three-transistor memory cell with aluminum gate p-MOS technology established dynamic RAM's at 1,024-bit complexity. With the development of the 1-T cell and silicon gate n-MOS technology 4,096-bit RAMs were established. Development of the 4k dynamic RAM also required improvements in the technology to detect the stored information. The small sense signals from the 1-T cell in complex memories ($\geq$ 4k) is a major concern in array design and processing control and is also the first-order effect in reducing their radiation hardness. Evolution from the 1k to 4k memories also included improvements in speed resulting from the application of self-aligned silicon gate n-MOS transistors rather than aluminum gate p-MOS transistors, reduction in clock signals and signal levels, and low-impedance TTL-compatible output drivers.

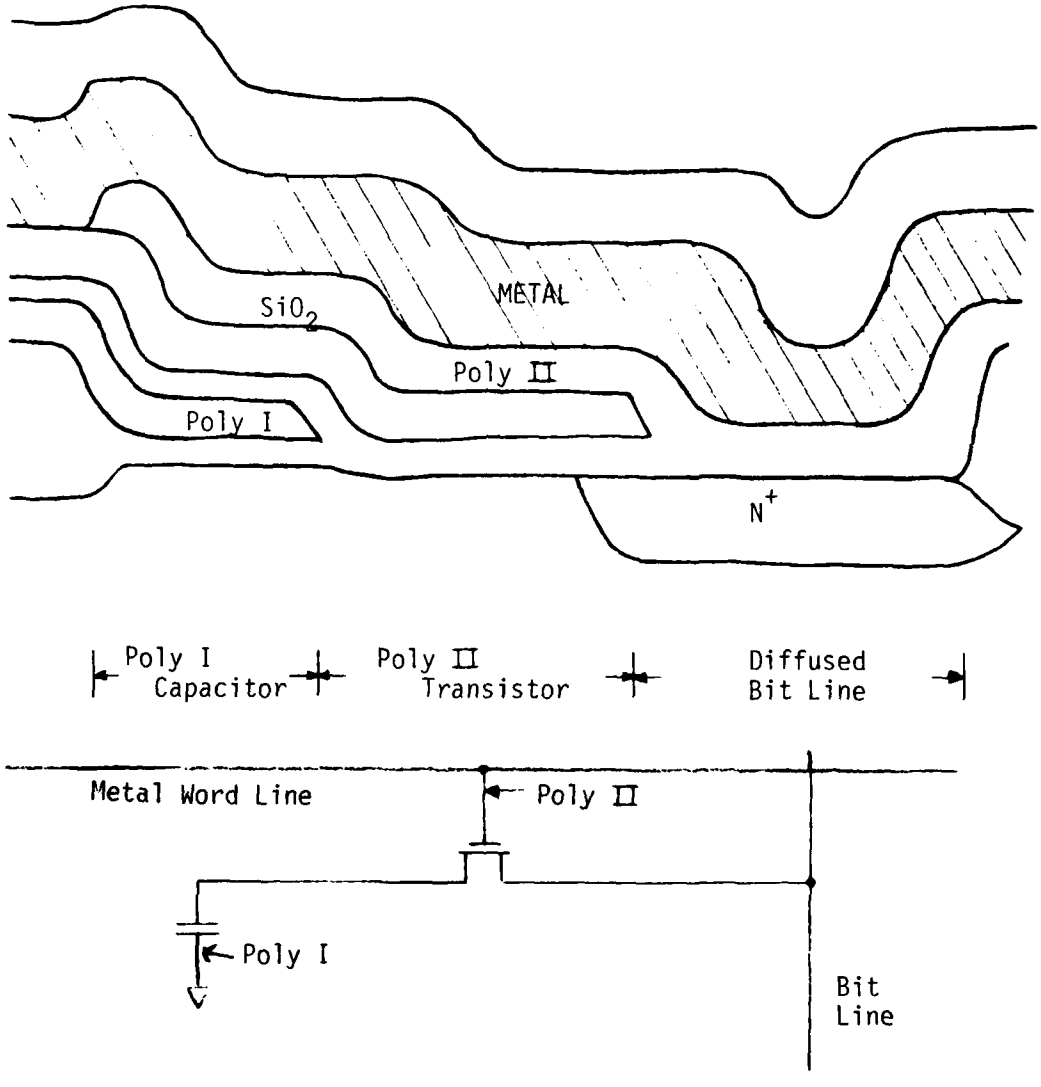
Further improvements in cell geometry can be realized by merging the transistor and capacitor elements of the 1-T cell into the same area. This can be accomplished by using two levels of polysilicon separated by oxide. The implementation of a two-level poly cell in a 16k dynamic array is shown in Figure 3.[9] The cell area of the single level poly cell used in the 4k memory is 1.01 mil^2 while the merged two-level poly cell has an area of 0.55 mil^2.[9]

The evolution beyond 16k dynamic RAMs was principally the result of scaling device geometry and gate oxide thicknesses. The principal of MOS transistor scaling is to increase switching speed by reducing the drain-source spacing.[10] To maintain the dc characteristics of the MOS transistor, all of the physical dimensions-channel length (L), gate-Oxide thickness (T_{OX}), junction depth (X_J), and lateral diffusion of the source and drains under the gate (L_D) — must be reduced by the scaling factor 1/K. At the same



3a. Mostek 16k RAM cell layout

Figure 3. 16k dynamic RAM memory cell.[9]



3b. Mostek 16k RAM cell and cross section.

Figure 3. 16 k dynamic RAM memory cell.[9]

time, threshold and punchthrough levels must be maintained by increasing the substrate doping concentration by a factor of K and reducing the power supply voltage by a factor of 1/K. The effect of scaling for one set of processing parameters is illustrated in Table 2. In practice, design parameters are adjusted somewhat to optimize performance and yield.

Table 2. Example of MOS scaling [4]

Parameter	"Std" Process	Scaled
Supply Voltage	12 V.	5 V.
Channel Length	5 μm	2.1 μm
Oxide Thickness	850 Å	354 Å
Substrate Resistivity	10 Ω-cm	6 Ω-cm
Junction Depth	1.2 μm	0.41 μm

The current state-of-the-art for dynamic n-MOS is apparently at 64k-bit arrays. These arrays are generally still in the research laboratories or pre-production. At this level of complexity it appears that scaling techniques are necessary which will require the "standard" 12 volt supply to be reduced to 5 volts. It can be argued that lower supply voltages would be desirable but there is intense resistance to maintain TTL 5 volt compatibility.[10] Unfortunately there are design parameters which do not readily scale. The capacitance and RC delays in conductive lines do not scale and is critical for complex RAMs. For example use of a refractory metal coating (e.g. molybdenum) on the poly-silicon is under consideration to increase the conductivity of the long critical bit lines. With the reduction in power supply voltage the amplitude of the cell signal at the sense amplifier will decrease from a level which is already too small. Diffusion and oxide capacitances at line edges and boundaries also do not scale and will limit array performance. A short-term realization for the 64k dynamic RAM can be the fabrication of four-16k arrays on a single chip (e.g., Motorola MCM6664).

A variety of new cell concepts have been proposed, all of which use sophisticated read/write signal processing and technology requirements.[11] It is not clear that a new cell will be necessary for the 64k RAM but the driving force may be the 256k-bit dynamic RAM.

2.1.2 n-MOS Static Memory Cell

The memory cell for a static n-MOS RAM is generally the six-transistor cell shown in Figure 4. The two cross-coupled inverters form a flip-flop with read/write access to the cell through the transmission gates. The load elements on the flip-flop switching transistors are depletion-mode n-MOS transistors. This memory cell has evolved in performance during the past few years as a result of device scaling. For example, Intel introduced the logic cell in this form in 1974 with the 2102A 1k RAM. While the principal objective of scaling has been to improve switching performance a substaintal gain has been realized in cell density. For example the cell area of the 2102A has been reduced from approximately 7 $mils^2$ to 3 $mils^2$. The static RAM capacity also increased from 1k bit to 4k bits.

Evolution beyond the 4k static RAM required an evolution in the cell circuit as well as device scaling. Polysilicon resistors were incorporated as the inverter loads as shown in Figure 5. The resistors are formed in a second level of polysilicon and the decrease in cell area is accomplished by locating the resistors over the active cell elements. Without device scaling the cell area was reduced to approximately 2 $mils^2$ (e.g., Mostek 4118 8k RAM[12]) and was reduced to 1.3 - 1.5 $mils^2$ using device scaling (e.g., Mostek 4801 8k RAM[12], Intel 16k RAM[13,14]).

2.1.3 CMOS Memory Cell

The typical CMOS memory consists of the six-transistor cell, as shown in Figure 6, using two cross-coupled CMOS inverters and two transmission

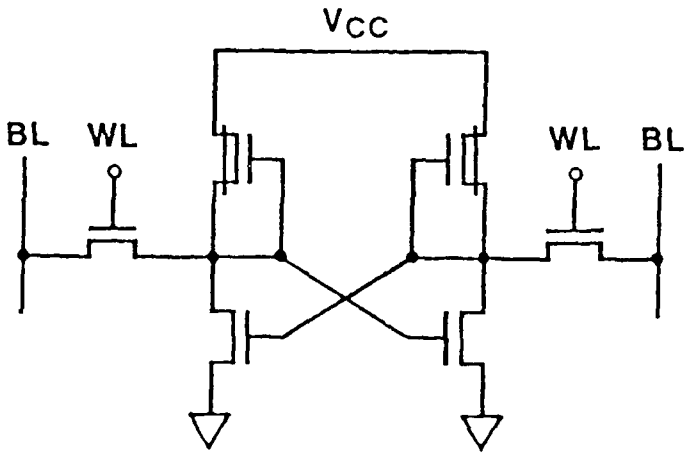


Figure 4. Depletion load static n-MOS memory cell.

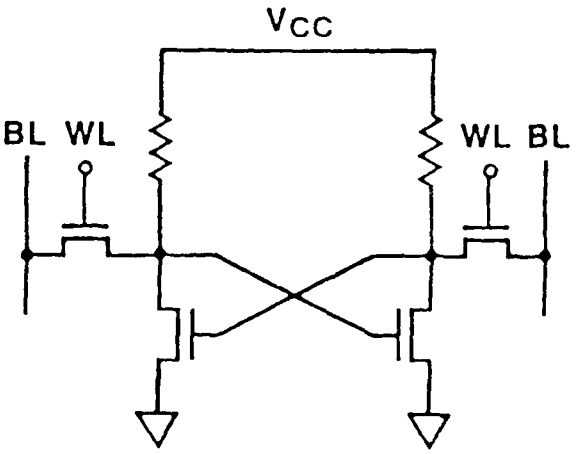


Figure 5. Poly resistor load static n-MOS memory cell.

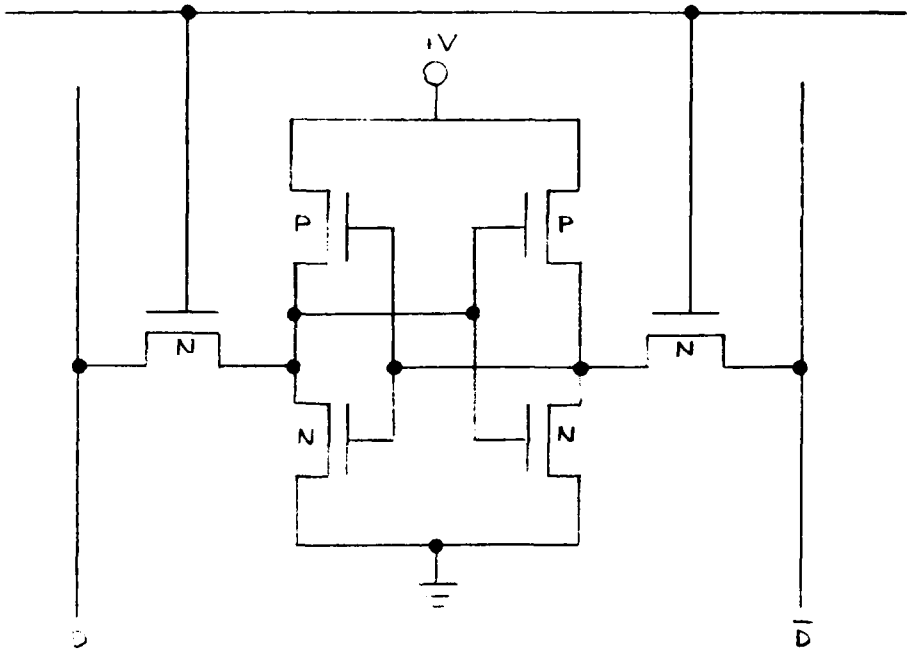


Figure 6. Six transistor CMOS RAM cell.

gates for coupling read/write data. The six-transistor cell is somewhat larger than the 6-transistor static n-MOS cell because of the area required for the p-well of the n-MOS transistors and the n^+ guard band. For the same layout rules, the 6-T CMOS cell requires about 1.5 times the area of the 6-T n-MOS cell.[15] A more compact form of a CMOS memory cell can be realized with the five-transistor cell as shown in Figure 7. The area required for the 5-T CMOS cell requires about 1.2 times that of the 6-T n-MOS cell.[15] The gain in density is offset by substantially greater difficulty in writing information into the cell.

2.1.4 Bipolar Memory Cells

The typical memory cell in a modern high-speed array is the emitter-coupled cell shown in Figure 8. The collector load resistors define a sufficient voltage differential to latch the flip-flop while the cell is biased with the low (typically 10 μA) standby current. The voltage drop across the load resistors must, however, be small enough to avoid a significant forward bias on the load by-pass diodes. When the memory cell is selected the bit line current is increased (typically, 300 μA), the load bypass diodes are forward biased and the cell switches with the speed of low-resistance collector loads. The principal disadvantage of the cell is the chip area required to realize the high-value load resistors. Limits on the resistance value require higher standby cell current to keep the flip-flop latched. A critical transistor parameter of the cell is the transistor gain requirement which is approximately equal to the ratio of selected bit line and standby current (approximately 30 for the typical 300 μA/10μA current levels).

Some of the limitations of the diode/resistor load cell can be mitigated by replacing the load resistors by pnp transistors as shown in Figure 9.

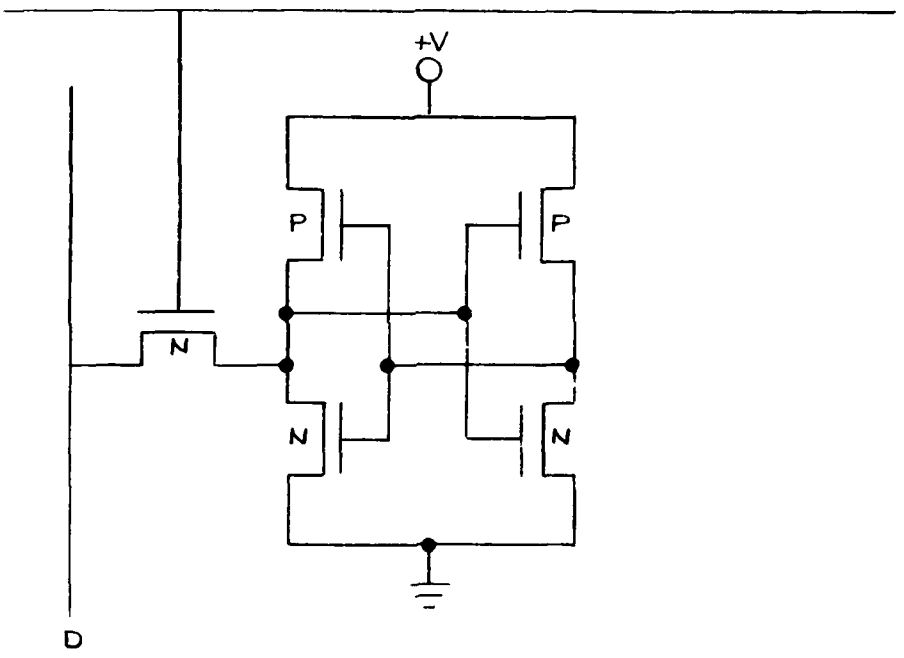


Figure 7. Five transistor CMOS RAM cell.

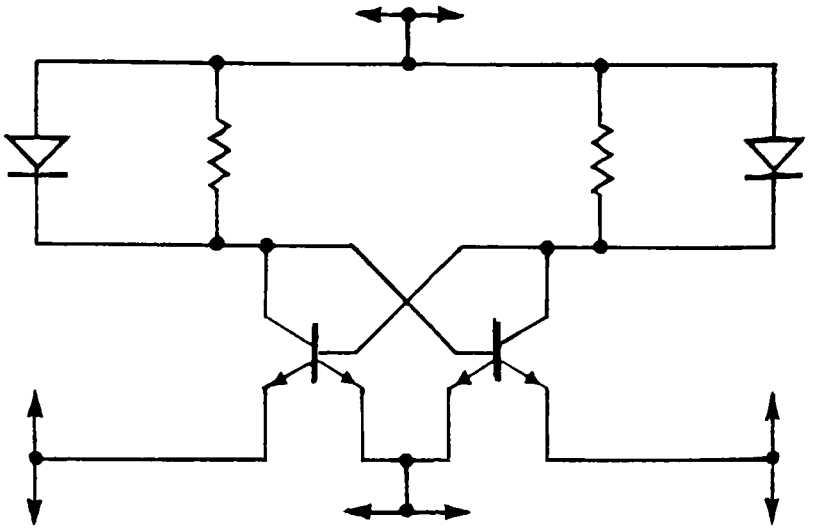


Figure 8. Bipolar ECL resistor coupled cell with diode bypass.

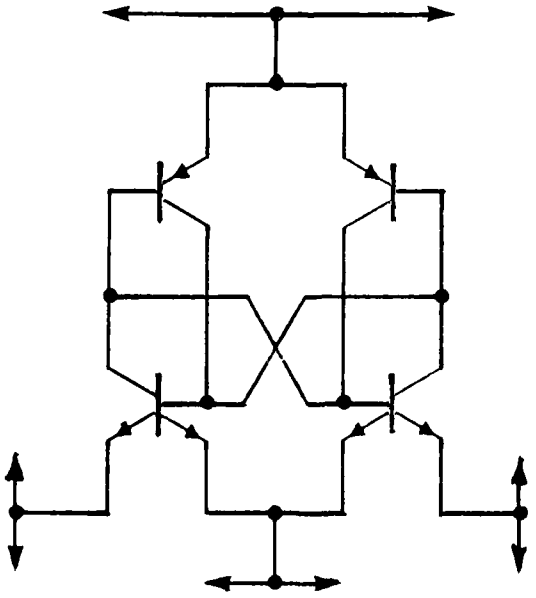


Figure 9. Bipolar ECL PNP coupled cell.

2.2 PERIPHERAL CIRCUITS

Although the most critical element of a Random-Access-Memory is the memory cell, the peripherical circuits are essential to the development of a successful array. The peripheral circuits include the address decoders to enable the selection of a specific cell, the write amplifier/drivers, the read sense amplifiers and the output drivers. In addition, specialized circuits may be required for specific technologies such as the substrate-bias for single-supply-voltage n-MOS and on-chip clock generators, multiplexiers and latches for dynamic memory arrays.

It is difficult to assess the comparative impact of the peripheral circuits on the overall RAM performance. A rough measure of density is the overall chip area for a given RAM function but this can be obscured by subtle variations in design rules and priorities between overall features and/or performance parameters. In the following discussion I will comment on some of the critical considerations in the peripheral circuit as they impact memory organization and chip area.

2.2.1 Address Decoders

Two schemes can be used for memory addressing: linear select or two dimensional (or x-y) select. In linear select each bit of the word is selected as one of a linear array. Other bits of the selected word are accessed simultaneously from parallel linear arrays. Linear select has the advantage that a cell can be activated with a single signal but has a formidable disadvantage in the required complexity of the address decoder network. For example a 1,024 words × 8-bit (8,192-bit) RAM requires 1,024 address lines, one for each 8-bit word. Thus a RAM must incorporate an on-chip 10- to 1,024-line decoder to keep the pins on the package to 10 for addressing. The number of gates necessary to realize the decoder would depend on the fan-in/fan-out for a specific technology, in any event the decoder network complexity would be a significant fraction of that of the memory cell array.

A substantial saving in the decoder complexity is realized by using two-dimensional addressing. In this scheme a selected cell is addressed by the coincidence of an x- and y-address word. Thus for each of the 1,024 elements of an array only two 1-of-32 address decoders would be required rather than the 10-to-1,024 required by one-dimensional addressing. The disadvantage of x-y decoding is that the memory cell must be selected by coincidence of the x- and y-signals. This is conveniently accomplished in MOS technology by transmission gates. Figure 10 shows the organization of such as that used in the 4k × 1 static RAM using the six-transistor cell shown in Figure 4. Two-dimensional selection of bipolar arrays is accomplished by gating and current switching. For the ECL memory cell, for example (Figure 8) the cell is selected by coincidence of word line and bit line signals. In general x-y decoding is less convenient for bipolar cells than MOS cells but the technique is used universally for all contemporary memory arrays in preference to one-dimensional selection.

2.2.2 Write Drivers

The write driver(s) must deliver enough energy to the selected cell to insure data storage. In large memory arrays long lines must be driven which increases the drive requirements on the write drivers. This non-scaling requirement dominates the trend of decreased storage energy requirements in the memory cells. Drive requirements impact the element geometry and circuit complexity of the write networks and they can occupy a significant portion of the chip area.

2.2.3 Sense Amplifiers

Next to the memory cells, the read sense amplifiers are the most critical circuits of the RAM array. In general, the sense amplifiers are located at the end of a long bit line. Thus the memory cell logic state is detected through a line of high capacitance and significant RC delay.

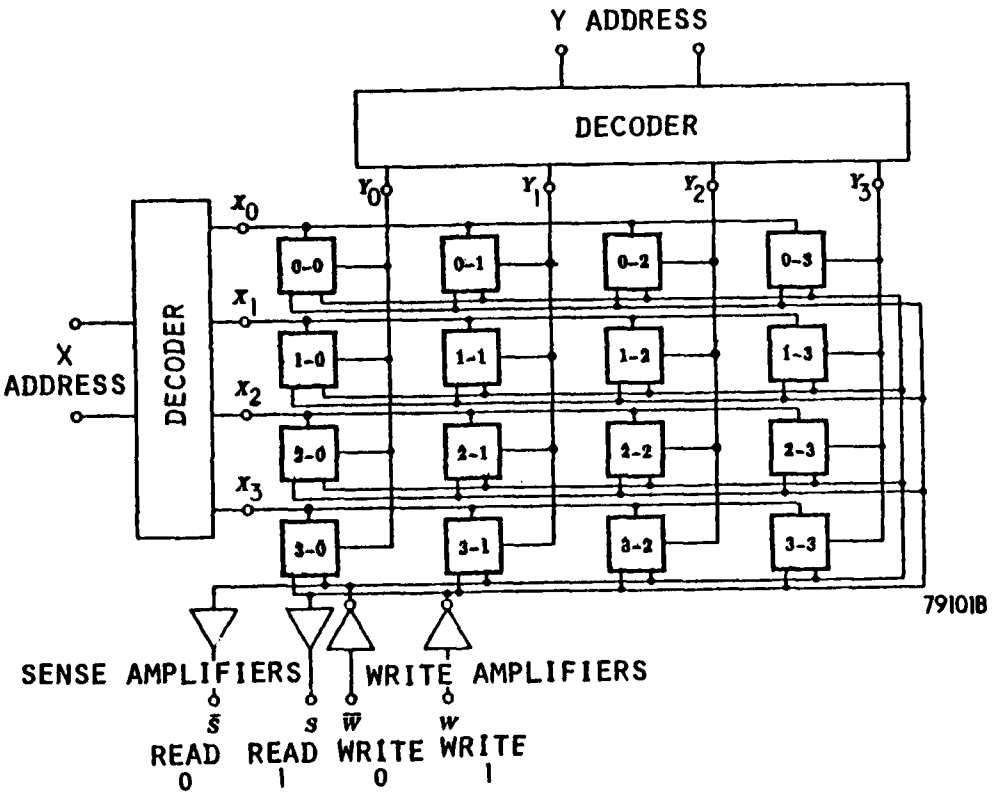


Figure 10. Two-dimensional address memory organization.

For example, the memory cells and dynamic sense amplifier of the Mostek 4116 dynamic 16k RAM are shown in Figure 11. When the bit line is selected the capacitance of the cell appears in parallel with the capacitance of the bit line. Since the bit line capacitance is on the order of 30 times that of the memory cell the voltage level on the parallel capacitance drops to (1/30)th of the memory cell voltage. For a logic-one voltage level of 12 volts on the memory cell the resultant signal at the sense amplifier will be 400 mV. In this case the threshold voltages on transistors T_1 and T_2 are matched to within 140 mV to insure accurate data resolution.

The impact of the sense amplifier design on the memory array organization and required area is in the required complexity of the sense amplifier circuit and definition of minimum signal levels. The minimum signal levels requirements impact memory cell layouts such that bit line lengths are minimized and impact design signal levels of memory cell operation.

2.2.4 Interface Circuits

The output drivers must transform the signal energy levels of the array to the energy levels of data stored on the capacitance of interpackage and inter-board wiring. The energy required for a 5V. "TTL" signal on a 39 pF output line is 375 pJ. This is in contrast to the 1-10 pJ energy committed to information storage in a large, low-power RAM. Thus, the output gain requirements and drive capability are significant. Bipolar arrays are generally at an advantage in terms of output drive capability because of better transconductance than MOS elements for transistors of comparable area. Of bipolar technologies, I^2L is somewhat limited because of the limited gain of the "inverted" transistor element. Of the MOS technologies CMOS or n-MOS/SOS is limited because of the reduced carrier mobility in the thin silicon film compared to that of bulk silicon. Output driver circuits can be realized in all cases but with variations in the required chip area.

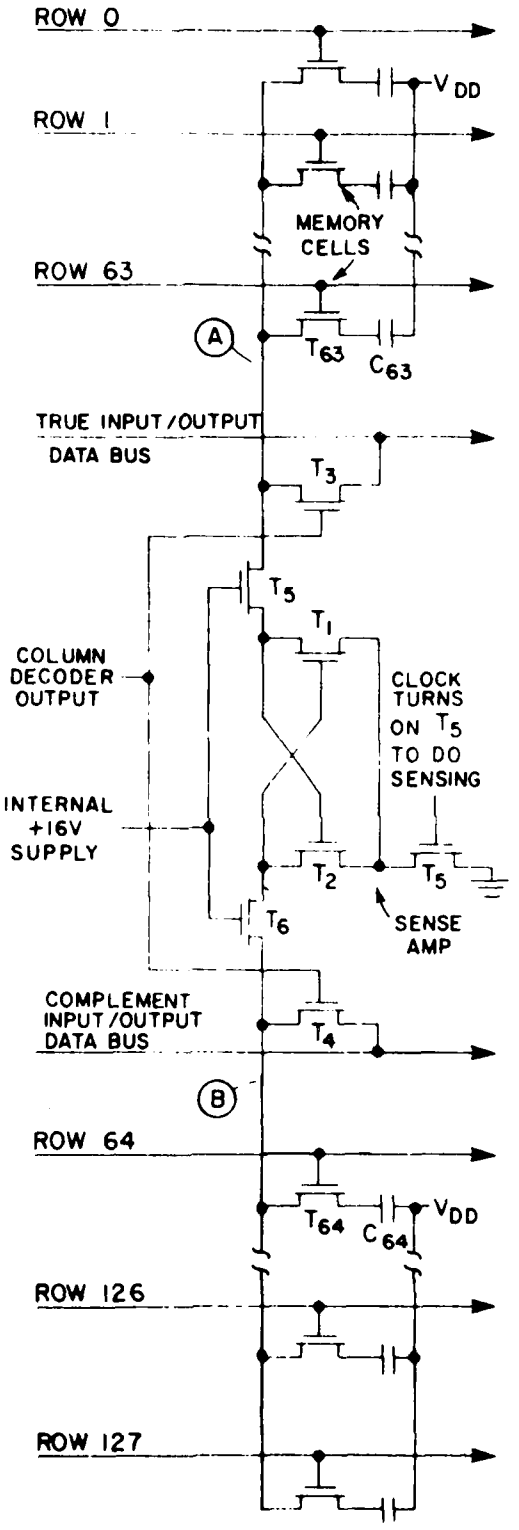


Figure 11. 16k RAM memory cells and dynamic sense amplifier.

Desirable interface characteristics presently include compatibility with TTL voltage and current requirements as well as tri-state outputs in which operation of a variety of microcircuits can be fed into a common line with each contributing data individually as they are selected. These interface requirements generally result in additional circuits on the chip which may be of significant complexity in some cases.

2.2.5 Support Circuits

Dynamic RAMs require carefully controlled timing in signal flow and data refresh. In every new memory design a portion must be defined between external chip and on-chip timing circuitry. In general it would be nice to do as much timing on-chip as possible but chip area is limited. External chip signals, on the other hand, require additional pins on the package and user responsibility to provide correctly timed signals (both of which build up sales reluctance).

A support circuit unique to n-MOS arrays is the substrate bias generator used on those arrays employing a single +5V. power supply. The substrate reverse bias for threshold voltage control on the transistor elements and to prevent diode saturation/recovery on input signals with small (i.e., 200 mV) negative voltage excursions.

2.3 TECHNOLOGY COMPARISON

Chip areas of selected RAMs are summarized in Table 3. It was attempted to select arrays of a common organization and contemporary technology. In most cases a 4,096 word x 1 bit array was a reasonable common denominator. The exception was the 16k dynamic n-MOS RAM. There was no data on a 4k RAM of 1979 fabrication technology to be comparable with the other arrays.

Table 3. RAM chip area comparison.

Manufacturer/Type	Size	Technology	Chip Area
Mostek 4116	16,384 × 1-bit	dynamic n-MOS	14.4 mm^2
Intel 2147H	4,096 × 1-bit	static n-MOS	13.7 mm^2
Harris HM6504	4,096 × 1-bit	CMOS	19.4 mm^2
AMI	4,096 × 1-bit	VMOS	6.7 mm^2
RCA	4,096 × 1-bit	CMOS/SOS	15.5 mm^2
Fairchild F10470	4,096 × 1-bit	bipolar ECL	8.0 mm^2
Fairchild	4,096 × 1-bit	bipolar TTL	15.5 mm^2
Fairchild 93481	4,096 × 1-bit	bipolar, dynamic I^2L	7.6 mm^2

All the considerations previously discussed should be considered in interpreting the relative chip areas. The following observations, however, may represent interesting trends.

Scaling the 16k dynamic RAM by a factor of two would suggest it as the smallest area of the production technologies. This seemed somewhat surprising. The memory cell geometry is certainly minimum but extensive and complex support circuits are required for the dynamic timing and refresh. The smallest 4k array is the AMI VMOS which may be ahead of its time and has been withdrawn from production. Exclusive of the 16k dynamic n-MOS, the smallest production 4k array is the bipolar ECL RAM. This is somewhat surprising because of the relatively large memory cell. Even smaller is the bipolar dynamic I^2L RAM but, while more mature than the VMOS technology, it is not the category of mature production technology (e.g., no second-source availability). Chip area of the static n-MOS array is almost twice that of VMOS, but is smaller than that of CMOS/SOS, TTL or CMOS arrays. The bipolar and CMOS/SOS arrays are of equal chip size. This is somewhat surprising because of the relatively large TTL memory cell area. The largest chip is that of the junction-isolated MOS RAM at about 1.4 times that of the static n-MOS array.

SECTION 3

ELECTRICAL SWITCHING RESPONSE/POWER DISSIPATION

Clearly, the goal in all RAM development is to maximize the rate of data processing. Generally, high speed is related to high power dissipation and bipolar technologies have traditionally led in both high speed and high power dissipation. Reduced n-MOS geometries have recently produced arrays which challenged bipolar speed at significantly lower power levels. The bipolar counterattack has also used geometry-reducing scaling techniques to realize high-speed ECL arrays in high-capacity RAMs. At the moment it appear that the fastest of bipolar technology still has the speed edge but the gap between technologies seems to be decreasing.

Electrical switching response seems to be specified in three (or less) general categories. The first is the read access time which can be defined as the delay time between the definition of a cell address and the appearance of valid data at the output(s). The second is the read or write cycle time. This is the delay time required to complete a read or write operation. The third is called the read-modify-write cycle time. This is the time required to read information in a specified memory cell and write revised information. In addition there is the chip select time, or the time required to bring the chip from unselected to active operation.

The specifications on switching operations of RAMs run from relatively straightforward on static arrays to incredibly complex for some dynamic arrays. There is a desire to simplfy system overhead in terms of

signal generation by either the development of static arrays, or the implementation of complex timing functions on-chip to make the complexity transparent to the user.

The most common specification of RAM switching response seems to be the access time. Response times as specified from manufacturers' data are summarized in Table 4. I have tried to be consistent in quoting the typical response of the arrays selected for fastest response.

Power dissipation is a much more critical parameter than just suggested by the system power requirement. The ability to draw heat from the semiconductor chip is limited. This limit is on the order of 500 to 1,000 mW without specific external cooling. Power dissipation of each cell must then be decreased as the array capacity is increased. For a 16,384-bit array the maximum power dissipation in each cell must be significantly less than 61 μW. For a 65,536-bit array it must be less than 15 μW for each memory cell.

Comparison of RAM switching response and power dissipation is difficult because of variations in operation between array type and the obfuscation of the manufacturers' specmanship. The switching response involves the variety of operations which must be performed as well as their associated time delays. These operations are very complex for a dynamic RAM. An experimental comparison would have been more helpful but there would still be significant uncertainty on system support overhead requirements. The issue of power dissipation is equally complex, principally because of the variations with operation mode and operating speed. In older static RAMs the power dissipation was essentially constant (i.e., independent of operating mode or speed). As array size increased power dissipation of individual circuit functions had to be decreased. The best way was to virtually eliminate current drain except when logic devices were switching the charge had to be transferred on capacitances. CMOS and CMOS/SOS

Table 4. Summary of RAM switching response.*

	Chip Select Time	Read Access Time	R/W Cycle Time	Read-Modify-Write Cycle Time	Refresh Period
Mostek 4116-2, 16k, dynamic n-MOS	100 ns	150 ns	320 ns	320 ns	2 ms
Intel 2147H,** 4k static n-MOS	22 ns	22 ns	32 ns	?	----
Harris HM6543, 4k CMOS	300 ns	70 ns	475 ns	?	----
Fairchild F10470 4k bipolar ECL	10 ns	30 ns	50 ns	?	----
Fairchild 93481 4k dynamic I^2L	?	100 ns	240 ns	?	2 ms

* values quoted are manufacturers' specification for production arrays except as noted.

** presented pre-production value, ? indicates value not specified

technologies employ this technique and minimize power dissipation at low operating speeds. Dynamic techniques (MOS and bipolar) use the same principle but with less effectiveness. Power dissipation of static arrays is generally independent of operating speed but can be a strong function of operating mode.

An additional complexity in the development of technology is the merger of dynamic and static technologies on the same chip. The Mostek 4104 1,024 word × 4-bit RAM, for example, uses static memory cells but dynamic peripherial circuitry.

Operating modes of the RAM which influence power dissipation can be defined as follows:

a) unselected — a chip with a tri-state output can be directly connected to a data bus. A signal (chip-enable) defines the active or passive operation of the chip. Unselected the output is a high impedance which does not load the data bus, and chip power dissipation can be minimized to the minimum level necessary to retain stored information. Selected, the chip drives the information bus and the operating power must be increased accordingly.

b) standby/inactive — the chip is selected but is not in active operation. This can either reflect a power-down mode or active operation at a very low data rate, depending on the technology and its associated specsmanship.

c) active — operation at maximum data rate. It is not clear that the specified represent a worst-case mixture of operating modes in terms of system requirements.

Power dissipation, as specified by array manufacturers, are summarized in Table 5 for selected RAMS.

Table 5. Summary of RAM power dissipation.*

	Operating Mode	
	Standby/Inactive	Active
Mostek 4116, 16k dynamic n-MOS	20 mW	462 mW
Intel 2147H, 4K** static n-MOS	45 mW	500 mW
Harris HM6543, 4k CMOS	1 mW	35 mW
Fairchild F10470 4k, bipolar ECL	?	1,000 mW
Fairchild 93481 4k, dynamic I^2L	45 mW	500 mW

* values quoted are manufacturer's specification for production arrays except as noted

** presented pre-production value

? indicates value note specified

SECTION 4
NOISE IMMUNITY

Noise immunity is a critical system parameter but difficult to define accurately. Three general categories can be defined for the purposes of discussion: 1) interface noise immunity,[16] 2) system noise immunity[16] and 3) soft errors.[17,18]

Interface noise immunity is critical for input signals on data, address or clock lines. For most RAM technologies interface circuits must be used to increase the noise immunity from the internal cells to the interface. One of the major advantages of LSI is designer control of the internal cell noise environment which allows a substantial decrease in signal levels and noise margins from those acceptable at the array external terminals. This trend will continue as the signal levels and information of the memory cells continue to decrease with increasing array complexity. In general, the interface circuits for both bipolar and n-MOS are designed to provide TTL characteristics and noise immunity ($\sim$ 300 mV). An exception to the general trend are CMOS and CMOS/SOS arrays. In this case the voltage noise immunity of the basic circuits is about 40% of the supply voltage ($\sim$ 2 Volts) and minimizes the requirement for special interface circuits.

System noise immunity can be defined as the noise generated by the array from internal current switching and generally appearing as current pulses in the power supply line. The magnitude of the power supply current transients and the supply voltage sensitivity of a technology determine system power supply current capability and required voltage regulation. Power

supply current surges occur in CMOS technologies and bipolar TTL during logic switching. During this time both transistors of the totem-pole inverter are turned on with a resulting supply current pulse. This current transient is relatively small contribution to TTL power dissipation but is the dominant component of CMOS and CMOS/SOS power dissipation. Similar current transients occur during switching operations in dynamic n-MOS RAMs.[19] Figure 12 shows the current transients illustrated by the manufacturer of the Mostek 4k dynamic RAM.

The third category of RAM noise immunity is "soft error" susceptibility. A soft error is defined as a loss of stored information without any permanent cell damage. The correct information can be rewritten into the RAM and stored with no degradation. Soft errors, of course, occur on a massive scale during exposure to high intensity pulsed radiation but that is typically referred to as transient upset. Soft errors, on the other hand, are the result of relatively localized ionization in the semiconductor caused by penetration of a high energy alpha particle or cosmic ray.

The soft error problem became apparent with the application of 4k dynamic n-MOS RAMs. The total charge committed to information storage was less than the induced ionization in the critical volume of the memory cells. Alpha particles causing the soft errors are emitted from trace radioactive materials in the device package. Improvements can be expected from improved packaging by either shielding the silicon chip or reducing "hot" impurities in the material. One of the major difficulties is measuring the extremely small amount of radioactivity in the package. The RAM itself is essentially a state-of-the-art detector for the low-level alpha emission.

Dynamic n-MOS arrays are generally the most susceptible RAMs to soft errors because of their dependence on charge storage in a very small semiconductor volume. I feel that the next most susceptible RAM technology is static n-MOS using polysilicon load resistors followed by the high load

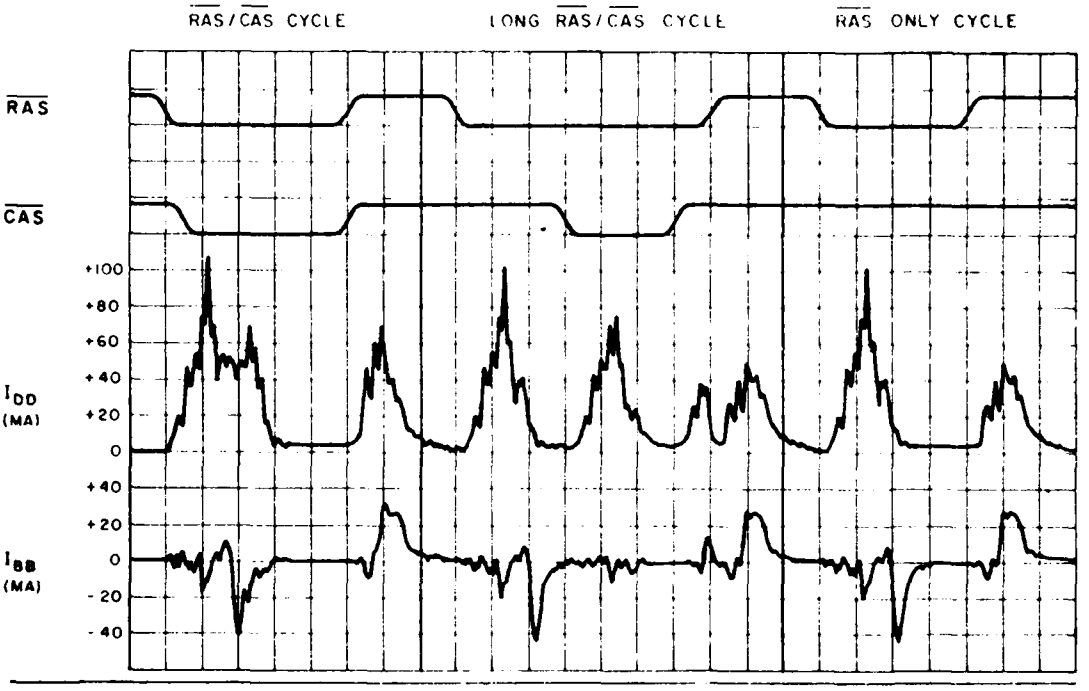


Figure 12. 4k dynamic RAM switching transients.[19]

resistance bipolar ECL cells, dynamic I^2L, and CMOS. Because of the high internal noise immunity and minimum semiconductor volume, I believe the CMOS/SOS arrays are essentially immune to soft error problems.

My relative evaluation of noise immunity for RAM technologies is summarized in Table 6. The notation of "good" refers to high noise immunity or low susceptibility and conversely for the notation of "poor".

Table 6. Subjective summary of RAM noise immunity.

	Interface Noise Immunity	System Noise Immunity	Soft-Error Susceptibility
dynamic n-MOS	average (TTL)	fair	poor
static n-MOS	average (TTL)	good	fair
CMOS	good	fair	good
CMOS/SOS	good	fair	excellent
bipolar, ECL	average (TTL)	good	fair
bipolar, I^2L	average (TTL)	good	good

SECTION 5

RADIATION SUSCEPTIBILITY

Critical radiation effects in RAMs is the ionizing-radiation-induced threshold voltage shift in MOS transistors, neutron-induced gain degradation in bipolar transistors, neutron- and/or ionization-induced increase in junction leakage currents, and pulsed ionization-induced junction photocurrents. The radiation susceptibility of the RAM is determined by the worst-case parameter in terms of its radiation sensitivity and its allowable variation for adequate circuit performance. The critical trend in RAM technology seems to be dependent on tighter margins which will erode array hardness. Process and circuit design technology evolution historically has improved array hardness. That trend has been reversed with the development of I^2L and new processing techniques but I feel that the general trend will still favor improving hardness.

The most dramatic increase in radiation susceptibility has that of dynamic n-MOS RAMs and static n-MOS RAMs to a lesser extent. Failure levels of unhardened dynamic n-MOS RAMs are on the order of 500 to 5000 rads(Si).[20] This has not been an erosion in basic MOS transistor susceptibility since contemporary CMOS RAMs have failure levels of greater than 50,000 rads(Si) using comparable technology. The problem is principally in the increasing sensitivity of n-MOS arrays to transistor threshold voltage shifts. As discussed previously, substantial signal loss is encountered between the memory cells and sense amplifier inputs for all large n-MOS arrays. The resultant tolerance to threshold voltages shifts is on

the order of 150-200 mV. Radiation-induced threshold voltage shifts outside this range will cause sense amplifier/total array failure. In addition to the sense amplifiers, timing signals in the dynamic RAM are critically designed. Non-uniform threshold voltage shifts change the gate propagation delays and can cause timing failures. At low radiation levels the threshold voltage of n-MOS transistors will decrease, decreasing the gate propagation delay. Relative timing, however, is critical and non-uniform decrease in propagation delay can be as disastrous as an increase in overall propagation delay times.

The design threshold voltage in modern n-MOS arrays is approximately 0.7 Volt which is somewhat less than used previously (typically 0.9 - 1.4 Volts). The radiation-induced shift is typically negative due to gate trapped charge and then back positive due to interface states as shown in Figure 13. If the threshold voltage becomes negative the transistor is operating in the depletion rather than the enhancement mode and conducts substantial current at zero gate bias. This will result in a substantial increase in array power supply current and will reduce the operating noise margin. Array failure may be by either. Even if the threshold voltage does not go through zero, the effect of the interface states is also a decrease in channel conductivity which will increase gate propagation delay and reduce gate driving capability. Either of these may result in RAM performance failure.

The reduction in initial threshold voltage may have the effect of decreasing array hardness but I believe that no further reductions seem to be probable in the (near) future. The present margins seem to be at the limit of producibility and future technology evolution will have to depend on gains in lithography and/or processing control.

Radiation-induced increase in leakage current is presently a problem and most critical for dynamic n-MOS but is also critical for dynamic I^2L and is becoming critical for high resistance, low current MOS and bipolar

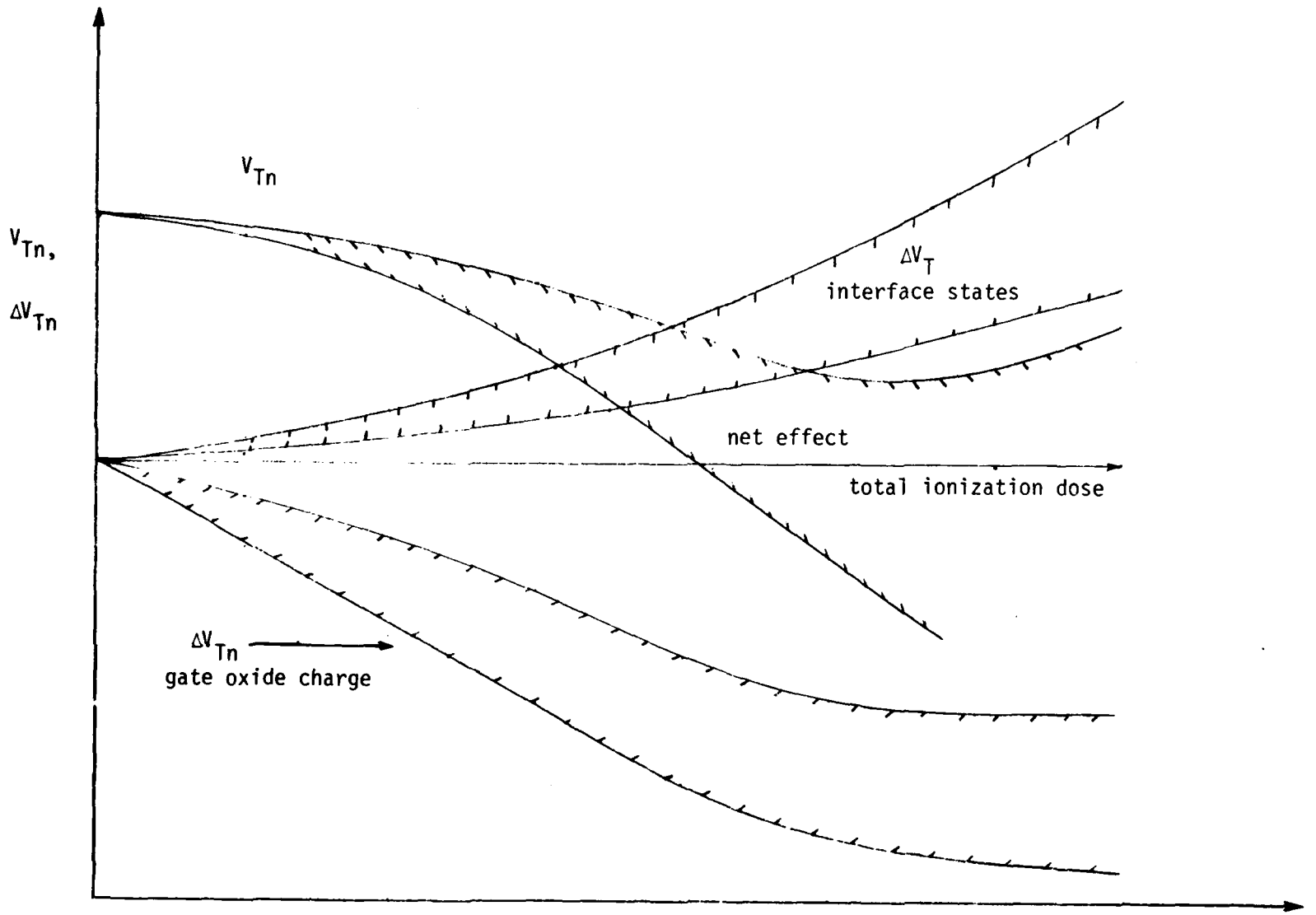


Figure 13. n-MOS threshold voltage ionization effects.

RAMs. Leakage current of the n-MOS transistor is critical in maintaining the extremely low standby power dissipation of CMOS and has been a major influence in hampering the development of hardened CMOS/SOS.

Neutron displacement damage effects are a second-order problem for MOS technologies (outside of the increase in leakage current) and no problem at all for CMOS/SOS. Susceptibility of MOS arrays is limited, however, by the concomitant ionizing radiation. Neutron displacement damage effects are, however, critical in bipolar arrays because of transistor current gain degradation. In older bipolar arrays the transistors were relatively hard and gain margins were very large with resultant neutron failure levels between 10^{14} - 10^{15} n/cm^2 (1 MeV equivalent). The development of I^2L brought the use of transistor operation unfavorable to neutron hardness and the radiation susceptibility of I^2L is on the order of 5×10^{12} to 5×10^{13} n/cm^2 (1 MeV equivalent). Even exclusive of I^2L there is a trend to depend on higher values of transistor gain than previously expected. In the ECL memory cell (Figure 8) the transistor gain required is approximately the ratio of the active/standby current which, in this case is a value of approximately 30. This is substantially greater than that formerly required in ECL or TTL circuits ($\sim$ 5-10) and may erode array hardness. Compensating for the increased gain requirement is the higher switching speed of the reduced geometry transistors.

An additional neutron exposure effect which may be critical in large RAM performance is neutron activation of package materials which may dramatically increase soft error rates, even at neutron fluences much lower than that required to cause critical displacement effects in the bulk semiconductor.

Transient effects in RAMs must be considered in terms of the radiation levels resulting in a variety of effects; the first the radiation level which causes a transient error in the output data but does not disturb

stored information, the second is the radiation level which disturbs the stored information and the third is radiation-induced latch-up. Critical upset levels and latch-up susceptibility have been extensively investigated for older logic arrays and RAMs. Dynamic n-MOS RAMs are the most susceptible and, based on dynamic shift register data, stored information may be lost for a pulsed radiation exposure of 1 rad(Si) during the refresh time (typically 2 ms). Logic upset levels for older static n-MOS and bipolar technologies are on the order of 5×10^7 to 5×10^8 rads(Si)/s. The critical pulsed radiation intensity is somewhat greater for CMOS ($\sim 10^9$ rads(Si)/s) and much greater for CMOS/SOS ($\sim 10^{10}$ - 10^{11} rads(Si)/s). Radiation-induced latch-up is a potential problem for junction-isolated technologies such as CMOS and TTL.

There is no data on transient upset levels and latch-up susceptibility of newly developed RAM technologies. The trend in technology is clearly toward devices of smaller geometry. This will reduce junction photocurrents which would increase hardness. On the other hand, signal current levels are being reduced and resistances increased which will decrease hardness. I feel that the balance of the trends will be a relatively small decrease in hardness with increasing RAM size. A more complex problem which may have a stronger effect on decreasing array hardness is the potential coupling between circuits and critical dependence on complex timing and on-chip bias circuits. As cell geometries decrease the spacing between cells may be small compared to the minority carrier diffusion length in the bulk semiconductor. Thus junction photocurrent effects may couple between circuits causing upset for very specific test conditions. It is possible that such effects could cause an operation latch-up in complex arrays independent of the familiar pnpn/SCR latch-up failure mechanism. In summary, the first-order upset susceptibility of current RAM technologies may decrease somewhat with arrays of increasing size but more subtle effects resulting from higher density and operational complexity may have a much more dramatic effect on reducing hardness and increasing the difficulty of worst-case test and analysis.

SECTION 6

CONSIDERATIONS FOR MILITARY SYSTEM APPLICATION

The technology selected for application must represent a balance between all electrical performance and radiation hardness parameters. Electrical performance requirements vary widely between systems depending on the priorities of speed, power dissipation, noise immunity, size and weight. Hardening requirements can be generally categorized into those of manned, satellite, boost missile and reentry systems. It is difficult to make general conclusions for broad military system applications. The following comments represent conclusions about trends in the RAM technologies that are worthy of consideration with specific system requirements.

In many ways it appears that the order of electrical performance advantages of RAM technologies is the inverse of that for radiation hardness. That conclusion is too strong. In terms of production technologies there are many advocates of dynamic n-MOS as the leader followed closely by static n-MOS. In terms of radiation hardness dynamic n-MOS is the most susceptible of all RAM technologies. It is expected that cointinuing evaluation of dynamic n-MOS will continue to have high radiation susceptibility and it is recommended that application in any hardened military system be subjected to critical review. Static n-MOS technology is somewhat less susceptible to radiation effects than dynamic n-MOS and has very impressive electrical performance capability. Current and evolving static n-MOS arrays are candidates for applications in manned systems and current hardening programs will provide needed margin above the manned system radiation requirements. Application to more systems with more severe radiation requirements should be critically reviewed.

The other two production RAM technologies are CMOS and ECL/bipolar. In both cases the same electrical performance parameters are at a disadvantage compared to the n-MOS technologies. However, CMOS is generally

preferred when power dissipation must be minimized and ECL which high speed performance is required. In terms of radiation hardness, ECL can be seriously considered for all hardened system applications. The application of CMOS is limited in hardened system application by its latch-up and total dose susceptibility. Processing variations have been demonstrated as effective in eliminating latch-up susceptibility. Assuming that latch-up free technology is employed (which is not necessarily assured by advertised "radiation-hardened CMOS") it is a candidate for all hardened system applications. At the present state-of-the-art hardness assurance sampling is required for all applications with the exception of manned systems.

RAM technologies under development include CMOS/SOS and I^2L. Both have impressive advantages in electrical performance and some aspects of radiation hardness compared to current production technologies. The critical questions for CMOS/SOS are producibility and total-dose hardness. The critical questions for I^2L are the development of a competitive RAM cell and neutron damage hardness. The total dose susceptibility of CMOS/SOS RAMs is of concern even for tactical systems. Total dose hardening could, however, bring the technology into consideration for all systems and particularly the very demanding requirements of reentry systems. Similarly the development of a competitive I^2L RAM cell would allow consideration for all hardened system applications. Most serious review would have to be for neutron damage effects of the reentry systems requirements.

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